What is claimed is:

1. A BZFLASH subcircuit configured to simulate alongside an impedance controlled buffer and provide BZ codes dynamically to the impedance controlled buffer, said subcircuit comprising:

a BZVREF subcircuit configured to provide a reference voltage equal to the I/O supply voltage divided by two;

a P_FLASH subcircuit configured to receive the reference voltage from the BZVREF subcircuit and configured to supply a plurality of binary output codes;

an N_FLASH subcircuit configured to receive the reference voltage from the BZVREF subcircuit, said N_FLASH subcircuit connected to said P_FLASH subcircuit and configured to supply a plurality of binary output codes to the P_FLASH subcircuit;

a first dither block connected to the N_FLASH subcircuit, said first dither block configured to receive a dither count and the plurality of binary output codes from the N_FLASH subcircuit and configured to subtract the dither count from the plurality of binary output codes received from the N_FLASH subcircuit and provide output codes in both a binary and a decimal voltage format; and

a second dither block connected to the P_FLASH subcircuit, said second dither block configured to receive a dither count and the plurality of binary output codes from the P_FLASH subcircuit and configured to add the dither count from the plurality of binary output codes received from the P_FLASH subcircuit and provide output codes in both a binary and a decimal voltage format.

2. A BZFLASH subcircuit as defined in claim 1, wherein said BZVREF subcircuit includes a resistive voltage divider between the I/O supply and ground.

3. A BZFLASH subcircuit as defined in claim 1, wherein said P_FLASH subcircuit includes a plurality of P_BIT_FLASH subcircuits which collectively output the binary output codes which are supplied to the second dither block.

4. A BZFLASH subcircuit as defined in claim 3, wherein each P_BIT_FLASH subcircuit includes a BZREFP subcircuit and a behavioral comparator which is configured to receive the reference voltage from the BZVREF subcircuit and an output signal from the BZREFP subcircuit.

5. A BZFLASH subcircuit as defined in claim 4, wherein each behavioral comparator is configured such that if the reference voltage which is received from the BZVREF subcircuit is greater or equal to the output signal received from the BZREFP subcircuit, then the behavioral comparator outputs VDD, and if the reference voltage which is received from the BZVREF subcircuit is less than the output signal received from the BZREFP subcircuit, then the behavioral comparator outputs VSS.

6. A BZFLASH subcircuit as defined in claim 4, wherein the BZREFP subcircuit includes a plurality of p-channel gates configured to receive a first set of inputs and a plurality of n-channel gates configured to receive a second set of inputs.

7. A BZFLASH subcircuit as defined in claim 1, wherein said N_FLASH subcircuit includes a plurality of N_BIT_FLASH subcircuits which collectively output the binary output codes which are supplied to the P_FLASH subcircuit and the first dither block.

8. A BZFLASH subcircuit as defined in claim 7, wherein each N_BIT_FLASH subcircuit includes a BZREFN subcircuit and a behavioral comparator which is configured to receive the reference voltage from the BZVREF subcircuit and an output signal from the BZREFN subcircuit.

9. A BZFLASH subcircuit as defined in claim 8, wherein each behavioral comparator is configured such that if the reference voltage which is received from the BZVREF subcircuit is greater or equal to the output signal received from the BZREFN subcircuit, then the behavioral comparator outputs VDD, and if the reference voltage which is received from the BZVREF subcircuit is less than the output signal received from the BZREFN subcircuit, then the behavioral comparator outputs VSS.

10. A BZFLASH subcircuit as defined in claim 8, wherein the BZREFN subcircuit includes a plurality of n-channel gates configured to receive a set of inputs and an input pad configured to receive a voltage input through an external reference resistor connectable to the input pad.

11. A BZFLASH subcircuit configured to simulate alongside an impedance controlled buffer and provide BZ codes dynamically to the impedance controlled buffer, said subcircuit comprising:

a BZVREF subcircuit configured to provide a reference voltage equal to the I/O supply voltage divided by two;

a P_FLASH subcircuit configured to receive the reference voltage from the BZVREF subcircuit and configured to supply a plurality of binary output codes;

an N_FLASH subcircuit configured to receive the reference voltage from the BZVREF subcircuit, said N_FLASH subcircuit connected to said P_FLASH subcircuit and configured to supply a plurality of binary output codes to the P_FLASH subcircuit;

a first dither block connected to the N_FLASH subcircuit, said first dither block configured to receive a dither count and the plurality of binary output codes from the N_FLASH subcircuit and configured to subtract the dither count from the plurality of binary output codes received from the N_FLASH subcircuit and provide output codes in both a binary and a decimal voltage format; and

a second dither block connected to the P_FLASH subcircuit, said second dither block configured to receive a dither count and the plurality of binary output codes from the P_FLASH subcircuit and configured to add the dither count from the plurality of binary output codes received from the P_FLASH subcircuit and provide output codes in both a binary and a decimal voltage format, wherein said BZVREF subcircuit includes a resistive voltage divider between the I/O supply and ground, wherein said P_FLASH subcircuit includes a plurality of P_BIT_FLASH subcircuits which collectively output the binary output codes which are supplied to the second dither block, wherein each P_BIT_FLASH subcircuit includes a BZREFP subcircuit

and a behavioral comparator which is configured to receive the reference voltage from the BZVREF subcircuit and an output signal from the BZREFP subcircuit, wherein each behavioral comparator in each P_BIT_FLASH subcircuit is configured such that if the reference voltage which is received from the BZVREF subcircuit is greater or equal to the output signal received from the BZREFP subcircuit, then the behavioral comparator outputs VDD, and if the reference voltage which is received from the BZVREF subcircuit is less than the output signal received from the BZREFP subcircuit, then the behavioral comparator outputs VSS, wherein the BZREFP subcircuit includes a plurality of p-channel gates configured to receive a first set of inputs and a plurality of n-channel gates configured to receive a second set of inputs, wherein said N_FLASH subcircuit includes a plurality of N_BIT_FLASH subcircuits which collectively output the binary output codes which are supplied to the P_FLASH subcircuit and the first dither block, wherein each N_BIT_FLASH subcircuit includes a BZREFN subcircuit and a behavioral comparator which is configured to receive the reference voltage from the BZVREF subcircuit and an output signal from the BZREFN subcircuit, wherein each behavioral comparator in each N_BIT_FLASH subcircuit is configured such that if the reference voltage which is received from the BZVREF subcircuit is greater or equal to the output signal received from the BZREFN subcircuit, then the behavioral comparator outputs VDD, and if the reference voltage which is received from the BZVREF subcircuit is less than the output signal received from the BZREFN subcircuit, then the behavioral comparator outputs VSS, wherein the BZREFN subcircuit includes a plurality of n-channel gates configured to receive a

set of inputs and an input pad configured to receive a voltage input through an external reference resistor connectable to the input pad.